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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,246	03/09/2004	Salman Akram	MIO 0069 VA/40509.245	2136

23368 7590 06/04/2007

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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	**PAPER NUMBER**
2813	

MAIL DATE	DELIVERY MODE
06/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,246	AKRAM ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,8,16 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,8,16 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/24/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed February 26, 2007.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098) in combination with Distefano (U.S. 6,075,289) and Fujisawa et al (US 6,184, 567).

4. Lo (Fig. 1) discloses:

(cl. 2, 23) a first semiconductor die (26) having a first active surface (i.e. top portion), said first active surface including at least one conductive bond pad (32); a second [*alternate first* for cl. 8] semiconductor die (40) defining a second active surface (i.e. bottom surface), said second active surface including at least one conductive bond pad (40a); a single intermediate substrate (12) comprising a network of conductive contacts (18) formed thereon, said substrate positioned between said first and second die, such that a first surface of said intermediate substrate (bottom) faces said first active surface and such that a second surface (top portion) of said intermediate substrate faces said second active surface (bottom portion), said intermediate substrate includes a passage (defined by item 24) and one of the first and second die active surface aligned with the

passage (i.e. die, 26), a printed circuit board (100) positioned such that a first surface (i.e. top portion) of the board faces the intermediate substrate; a plurality of topographic contacts (48) extending from said intermediate substrate to said first surface of said board; wherein said first die is electrically connected to the intermediate substrate by a topographic contact (52) extending form said first active surface to said intermediate with said second die secured (34) to the second surface of the intermediate substrate, such that the conductive pads (32) of the second die is aligned with the passage and said second die is electrically connected to the intermediate substrate by at least one conductive line (38) extending form the bond pad of the second die through said passage and to contact first surface of the intermediate substrate;

(cont. cl. 23) with at least one die bond pad (32) is aligned with passage.

5. Lo does not discloses a cap including a heat sink coupled to at least one die major surface with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate, or at least one decoupling capacitor mounted to an intermediate substrate and conductively coupled to at least one of said first and second semiconductor dies wherein said at least one decoupling capacitor comprises a thickness dimension (a), a die with a thickness (c), and a topographic contact extending between said intermediate substrate and one of the said first or second semiconductor dies, wherein said topographic contact comprises a thickness dimension (b) and said thickness dimension (a) is equal to or less than thickness dimension (b) or (c).

6. However, Distefano (Fig. 2) discloses a cap including a heat sink coupled to at least one die major surface (i.e. horizontal surface) with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate.

7. It would have been obvious to one of ordinary skill in the art to incorporate a cap including a heat sink to package of Lo in order to provide thermally enhanced packages as taught by Distefano (Title).

8. Neither Lo nor Distefano appear to show a capacitor with the claimed thickness as stated above.

9. However, Fujisawa (e.g. 13, 16) utilizes at least one decoupling capacitor (10) mounted to an intermediate substrate (e.g. 39, 43) and conductively coupled to at least one of said first and second semiconductor dies (40) wherein said at least one decoupling capacitor comprises a thickness dimension (a), a die with thickness (c), and a topographic contact extending between said intermediate substrate and one of the said first or second semiconductor dies, wherein said topographic contact comprises a thickness dimension (b) and said thickness dimension (a) is equal to or less than thickness dimension (b) or (c) [e.g., Fig. 16].

10. It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor onto the intermediate modified substrate of Lo such that said topographic contact comprises a thickness dimension (b) and said thickness dimension (a) is equal to or less than thickness dimension (b) or (c) as shown in Fujisawa in order to remove noise as taught by Fujisawa (Col. 1, Lines 31-34).

11. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098), Distefano (U.S. 6,075,289) and Fujisawa et al (US. 6,184,567) as applied to claim 2 and further in combination with Corisis et al. (U.S. 2002/0135066).

12. Neither Lo, Distefano nor Fujisawa appears to show its board is resident in a computer system, comprising a programmable controller, memory unit including board.

13. Corisis (Fig. 12) utilizes a board in resident in a computer system ("electronic system"; Par. 0024), comprising a programmable controller (132), memory unit including board (138).

14. It would have been obvious to one of ordinary skill in the art to incorporate the board of the prior art in a computer system comprising a programmable controller, memory unit including board in order to form an electronic system as taught by Corisis (Par. 0024).

15. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo et al. (U.S. 6,507,098) in combination with Distefano (U.S. 6,075,289), Fujisawa et al (U.S. 6,184,567) and Searls (U.S. 2004/0155335).

16. Lo discloses the elements stated in paragraph 4 of this office action, but does not discloses a cap including a heat sink coupled to at least one die major surface with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate, or at least one decoupling capacitor mounted to an intermediate substrate and conductively coupled to at least one of said first and second semiconductor dies wherein said at least one decoupling capacitor comprises a

thickness dimension (a), a die with a thickness (c), and a topographic contact extending between said intermediate substrate and one of the said first or second semiconductor dies, wherein said topographic contact comprises a thickness dimension (b) and said thickness dimension (a) is equal to or less than thickness dimension (b) or (c), or at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies or wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said first semiconductor die, said second semiconductor die, or a topographic contact, or connecting capacitor between high and low voltage inputs..

17. However, Distefano (Fig. 2) discloses a cap including a heat sink coupled to at least one die major surface (i.e. horizontal surface) with a peripheral portion that engages a mounting zone defined by lateral dimensions of the intermediate substrate.

18. It would have been obvious to one of ordinary skill in the art to incorporate a cap including a heat sink to package of Lo in order to provide thermally enhanced packages as taught by Distefano (Title).

19. Neither Lo nor Distefano appear to show a capacitor with the claimed thickness as stated above.

20. However, Fujisawa (e.g. 13, 16) utilizes at least one decoupling capacitor (10) mounted to an intermediate substrate (e.g. 39, 43) and conductively coupled to at least one of said first and second semiconductor dies (40) wherein said at least one decoupling capacitor comprises a thickness dimension (a), a die with thickness (c), and a topographic contact extending between said intermediate substrate and one of the

said first or second semiconductor dies, wherein said topographic contact comprises a thickness dimension (b) and said thickness dimension (a) is equal to or less than thickness dimension (b) or (c) [e.g., Fig. 16].

21. It would have been obvious to one of ordinary skill in the art to incorporate a decoupling capacitor onto the intermediate modified substrate of Lo such that said topographic contact comprises a thickness dimension (b) and said thickness dimension (a) is equal to or less than thickness dimension (b) or (c) as shown in Fujisawa in order to remove noise as taught by Fujisawa (Col. 1, Lines 31-34).

22. Neither Lo, Distefano or Fujisawa disclose attaching a capacitor between high and low voltages.

23. However Searls (Fig. 1; Par. 0067) utilizes disclose attaching a capacitor (130) between high and low voltages (118,140).

24. It would have been obvious to one of ordinary skill in the art to connect the modified package of Lo to include attaching a capacitor between high an low voltages in order to improve device performance as taught by Searls (Abstract).

Response to Arguments

25. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ex. Mitchell, J.D
May 29, 2007

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800